

V_{DSS} 60V

R_{DS}(on) 11.5m

I _D @ T _C = 25°C	$@ T_C = 25^{\circ}C$ Continuous Drain Current, V _{GS} @ 10V			
I _D @ T _C = 100°C	$_{\rm D}$ @ T _c = 100°C Continuous Drain Current, V _{GS} @ 10V		A	
Ідм	Pulsed Drain Current	200		
P _D @T _C = 25°C	Power Dissipation	65	W	
V _{DS}	Drain-Source Voltage	60	V	
V _{GS}	Gate-to-Source Voltage	± 20	V	
TJ TSTG	Operating Junction and Storage Temperature Range	-55 to +150	°C	



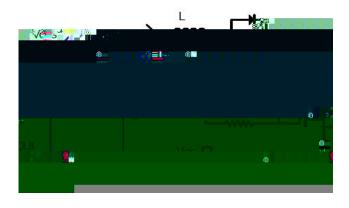
R JC	Junction-to-case	—	1.9	/W

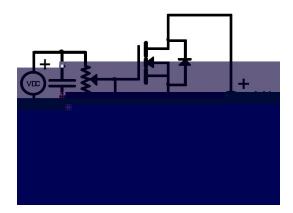
V _{(BR)DSS}	Drain-to-Source breakdown voltage	60		_	V	$V_{GS} = 0V, I_D = 250 \mu A$
R _{DS(on)}	Static Drain-to-Source on-resistance		11.5	15	m	V _{GS} =10V,I _D = 20A
V _{GS(th)}	Gate threshold voltage	2		4	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
I _{DSS}	Drain-to-Source leakage current			1	μA	$V_{DS} = 60V, V_{GS} = 0V$
I _{GSS}	Gate-to-Source forward leakage			100	nA	V _{GS} =20V
		_		-100		V _{GS} = -20V
Ciss	Input capacitance	_	1722			V _{GS} = 0V
Coss	Output capacitance	_	125		pF	V _{DS} = 25V
Crss	Reverse transfer capacitance	_	108			f = 1MHz
Qg	Total gate charge	_	37	_		I _D = 30A,
Q _{gs}	Gate-to-Source charge	_	6	_	nC	V _{DS} =30V,
Q _{gd}	Gate-to-Drain("Miller") charge	_	10	_		V _{GS} = 10V
t _{d(on)}	Turn-on delay time		15	_		
tr	Rise time		10	_		V_{GS} =10V, V_{DS} =30V,
t _{d(off)}	Turn-Off delay time		36	_	ns	R_{GEN} =1.8 , I_D = 30A
t _f	Fall time		29	_		

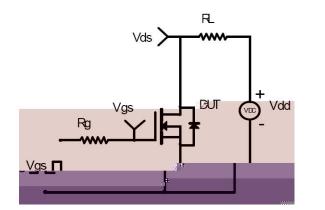
$@T_A=25$ unless otherwise specified

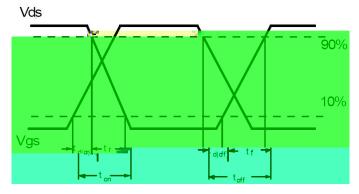
Is	Continuous Source Current		_	50	А	MOSFET symbol
	(Body Diode)					showing the
I _{SM}	Pulsed Source Current		_	200	А	integral reverse
	(Body Diode)	_				p-n junction diode.
V_{SD}	Diode Forward Voltage	—	_	1.2	V	Is=30A, V _{GS} =0V
trr	Reverse Recovery Time	—	38	—	ns	$T_J = 25^{\circ}C$, $I_F = 30A$, di/dt =
Qrr	Reverse Recovery Charge	—	50	_	nC	100A/µs









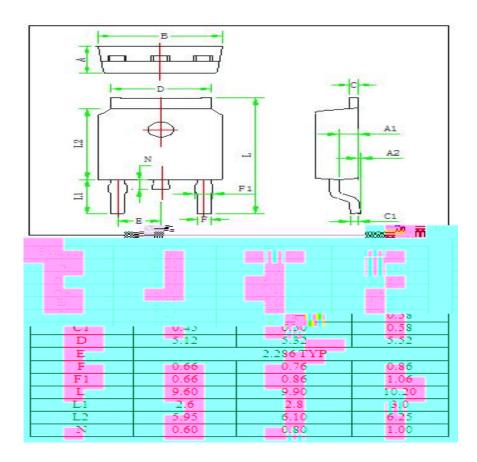


Calculated continuous current based on maximum allowable junction temperature.

Repetitive rating; pulse width limited by max. junction temperature.

The power dissipation P_{D} is based on max. junction temperature, using junction-to-case thermal resistance.







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