

SSF6072G5


Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
R	Junction-to-		38	/W
	Junction-to-Ambient (PCB mounted, steady-state)		35	/W

Electrical Characterizes @ $T_A=25$ unless otherwise specified

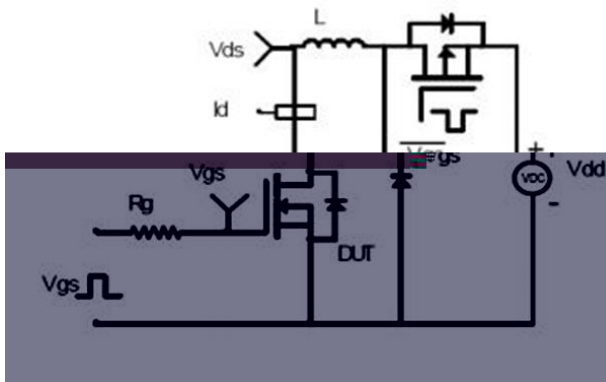
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60			V	$V_{GS} = 0V, I_D$
$R_{DS(on)}$	Static Drain-to-Source on-resistance		67	100		$V_{GS}=10V, I_D = 1.5A$
			76	115		$V_{GS}=5V, I_D = 1.5A$
$V_{GS(th)}$	Gate threshold voltage	1		2.5	V	$V_{DS} = V_{GS}, I_D = 250 A$
I_{DSS}	Drain-to-Source leakage current			1		$V_{DS} = 60V, V_{GS} = 0V$
				10		$T_J = 125^\circ C$
I_{GSS}	Gate-to-Source forward leakage			100	nA	$V_{GS} = 20V$
				-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	1			S	$V_{DS} = 15 V, I_D = 1.5A$
Q_g	Total gate charge		12		nC	$I_D = 4A,$ $V_{DS}=40V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge		3.5			
Q_{gd}	Gate-to-Drain("Miller") charge		3.7			
$t_{d(on)}$	Turn-on delay time		9.2		ns	$V_{GS}=10V, V_{DS}=25V,$ $R_{GEN}=50 \quad I_D = 1.2A,$
t_r	Rise time		16.7			
$t_{d(off)}$	Turn-Off delay time		35.4			
t_f	Fall time		8.6			
C_{iss}	Input capacitance		582		pF	$V_{GS} = 0V$ $V_{DS} = 30V$ 1MHz
C_{oss}	Output capacitance		49			
C_{rss}	Reverse transfer capacitance		36			

Source-Drain Ratings and Characteristics

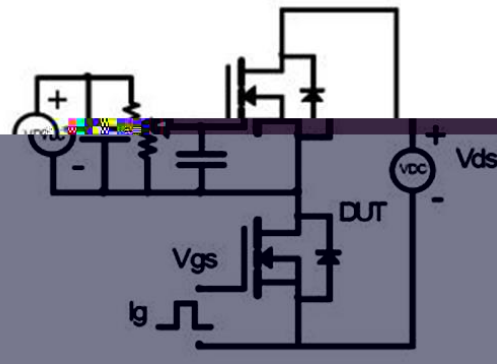
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)			4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)			16	A	
V_{SD}	Diode Forward Voltage			1.5	V	$I_S=4A, V_{GS}=0V$

Test circuits and Waveforms

EAS Test Circuit:



Gate Charge Test Circuit:



Switching Time Test Circuit:

Switching Waveforms:



Notes:

The maximum current rating is limited by bond-wires.

Repetitive rating; pulse width limited by max. junction temperature.

The power dissipation PD is based on max. junction temperature, using junction-to- ambient thermal resistance.

The value of R is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Typical Electrical and Thermal Characteristics

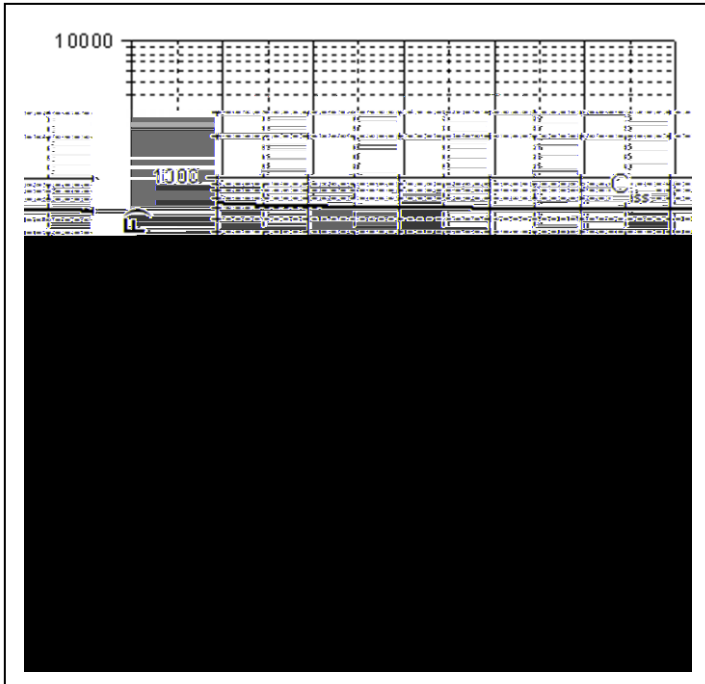


Figure 1. Typical Capacitance vs. Drain-to-Source Voltage

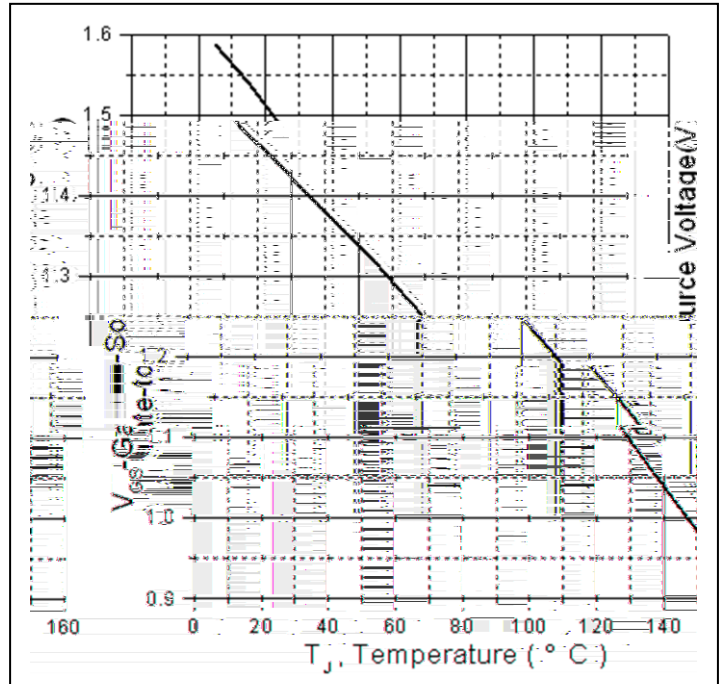


Figure 2. Gate to source cut-off voltage

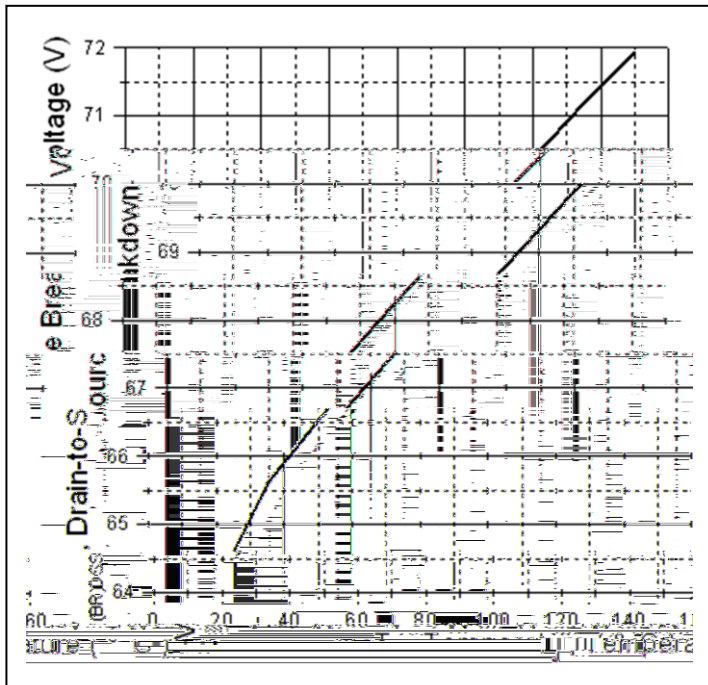


Figure 3. Drain-to-Source Breakdown Voltage vs. Junction Temperature

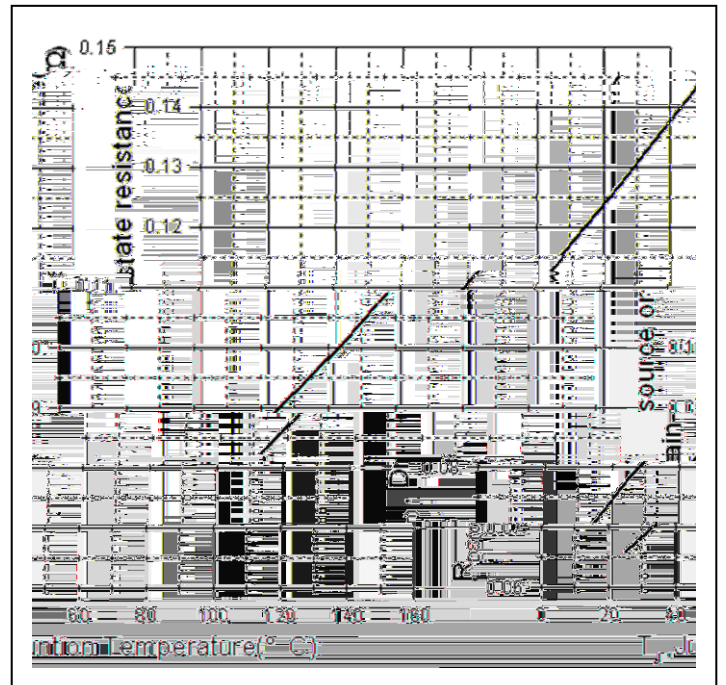


Figure 4. Normalized On-Resistance vs. Junction Temperature

Typical Electrical and Thermal Characteristics

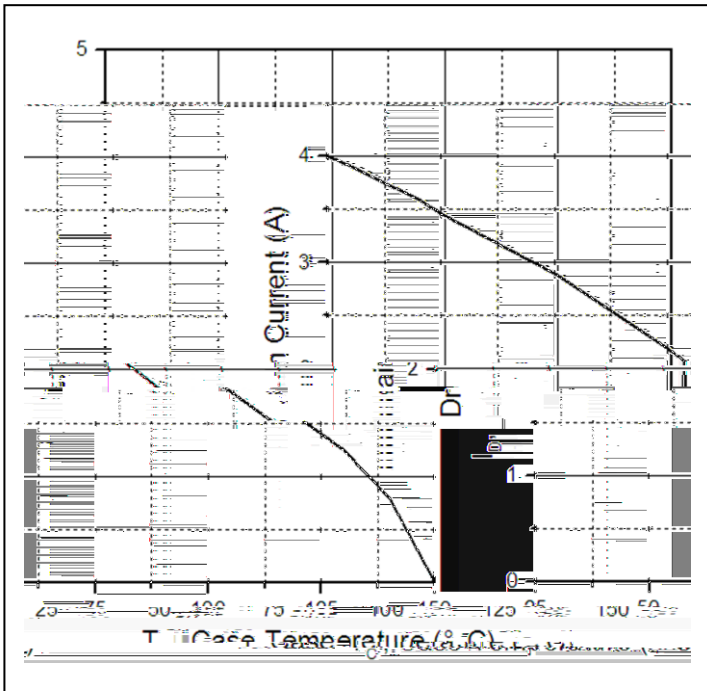


Figure 5. Maximum Drain Current vs. Case Temperature

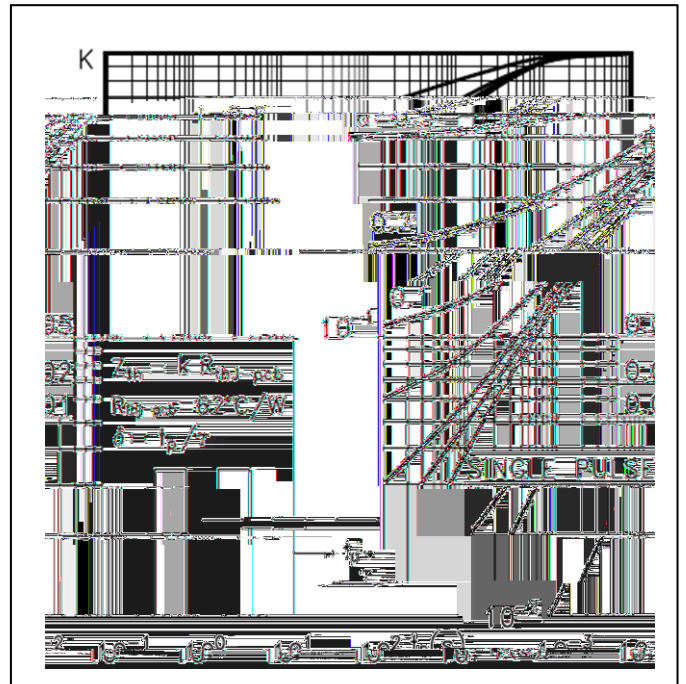
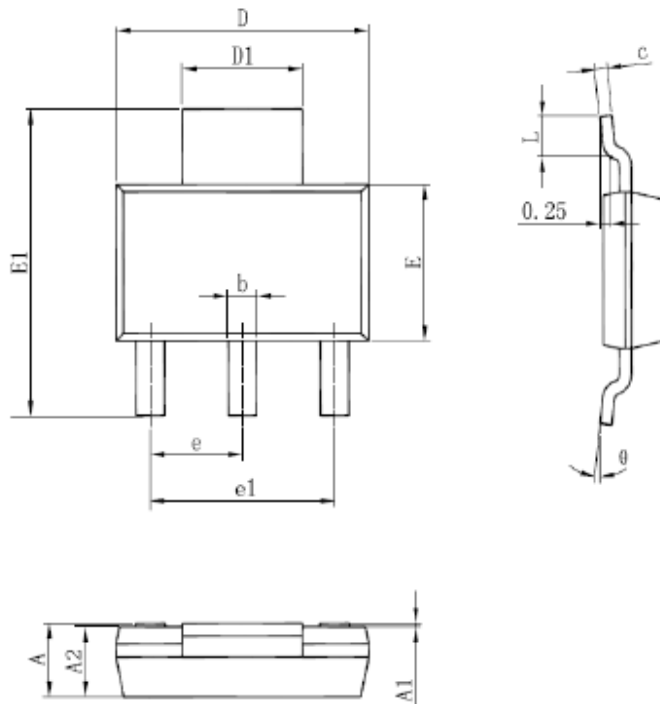


Figure 6. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

Option 1

SOT-223 Dimensions (UNIT: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.520	1.800	0.060	0.071
A1	0.000	0.100	0.000	0.004
A2	1.500	1.700	0.059	0.067

0.350	0.370	0.414	0.014	0.016
0.400	0.344	0.262	0.014	0.010
0.400	0.474	0.402	0.016	0.016
0.700	0.180	0.146	0.028	0.006
0.700	0.780	0.748	0.028	0.029
0.500	2.000(±0.050)	0.691(±0.050)	0.019	0.027
e	1.500	1.700	0.059	0.067
L	0.900	1.150	0.035	0.045

Notes

Dimensions are inclusive of plating

Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.

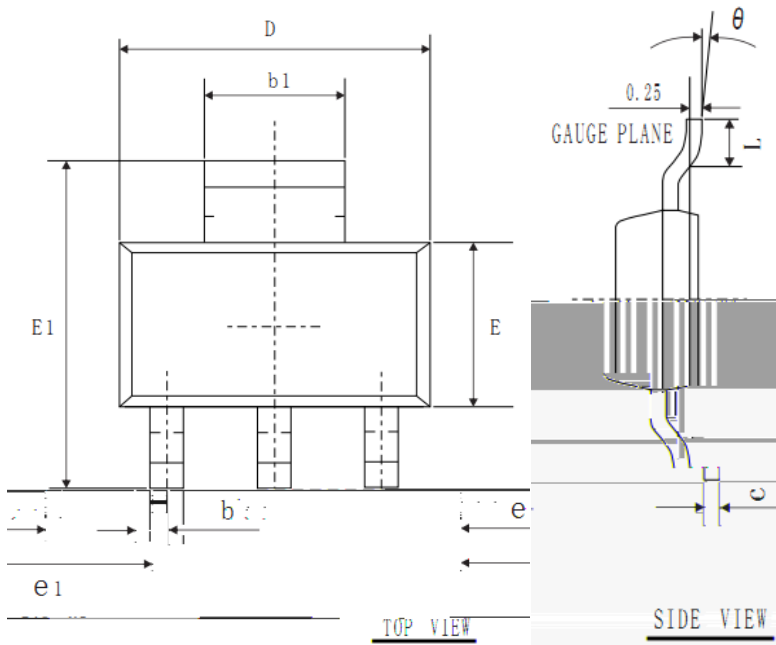
Dimension L is measured in gauge plane.

Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Mechanical Data

Option 2

SOT-223 Dimensions (UNIT: mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	DESCRIPTION	MIN	MAX	REFERENCE
A1	Lead length	0.80	1.00	A1
A2	Lead length	0.60	0.70	A2
A3	Lead length	0.90	0.95	A3
b	Lead width	0.20	0.25	b
c	Lead thickness	0.10	0.15	c
e	Lead pitch	0.50	0.50	e
E	Package height	0.80	0.85	E
E1	Package height	0.80	0.85	E1
e1	Lead spacing	0.50	0.50	e1
D	Package width	1.00	1.00	D
b1	Inner width	0.60	0.60	b1
theta	Lead angle	10°	10°	theta

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