Main Product Characteristics:

V_{DSS}	30V
R_{DS}(on)	25.8m (typ.)
I_D	5.8A

SOT-23

Schematic Diagram

Features and Benefits:

Advanced trench MOSFET process technology
Special designed for PWM, load switching and general purpose applications
Ultra low on-resistance with low gate charge
Fast switching and reverse body recovery
150 operating temperature

Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	5.8	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	4.2	
I_{DM}	Pulsed Drain Current	30	

Thermal Resistance

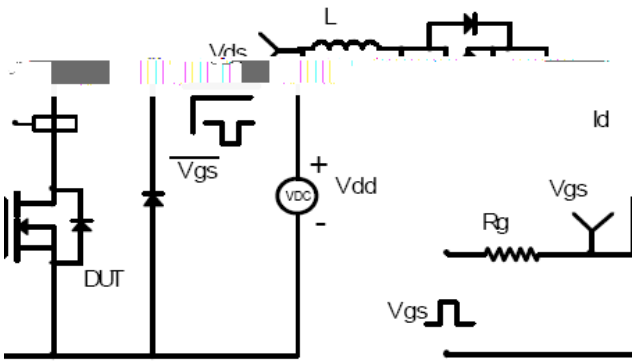
Symbol	Characterizes	Typ.	Max.	Units
R 90	Junction-to-ambient (t s)		145	/W

Electrical Characterizes @T_A=25 unless otherwise specified

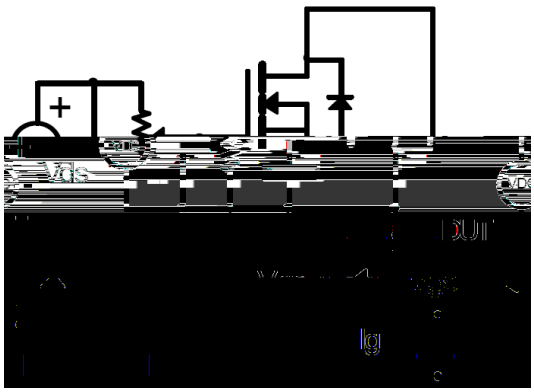
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	30			V	V_{GS} = 0V, I_D , A
$R_{DS(on)}$	Static Drain-to-Source on-resistance		25.8	30		V_{GS}=10V,I_D = 5.8A
			28.7	33		V_{GS}=4.5V,I_D=5A
			36.6	52		V_{GS}=2.5V,I_D =4A
$V_{GS(th)}$	Gate threshold voltage	0.7		1.4	V	V_{DS} = V_{GS} , I_D , 0
I_{DSS}	Drain-to-Source leakage current			1	A	V_{DS} = 24V,V_{GS} = 0V
I_{GSS}	Gate-to-Source forward leakage			100	nA	V_{GS} =12V
				- 100		V_{GS} = - 12V
Q_g	Total gate charge		11		nC	I_D = 5.8A,
Q_{gs}	Gate-to-Source charge		2			V_{DS}=15V,
Q_{gd}	Gate-to-Drain("					V_{GS} = 4.5V

Test Circuits and Waveforms

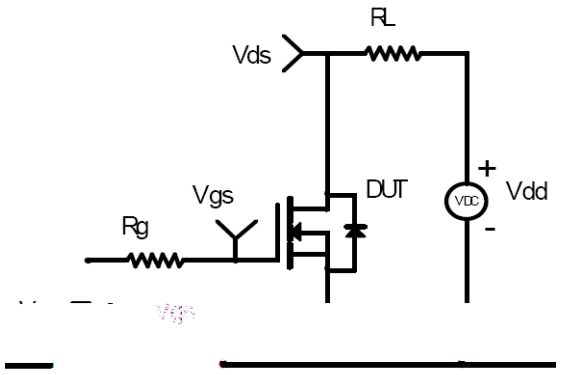
EAS Test Circuit:



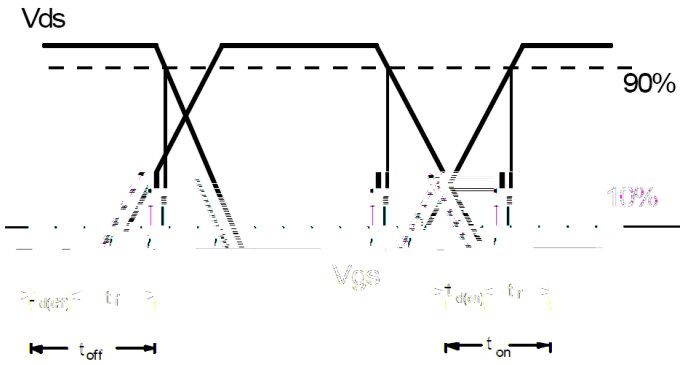
Gate Charge Test Circuit:



Switching Time Test Circuit:



Switching Waveforms:



Notes:

① Calculated continuous current based on maximum allowable junction temperature.

② Repetitive rating; pulse width limited by max. junction temperature.

③ The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal.

④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C

Typical Electrical and Thermal Characteristics

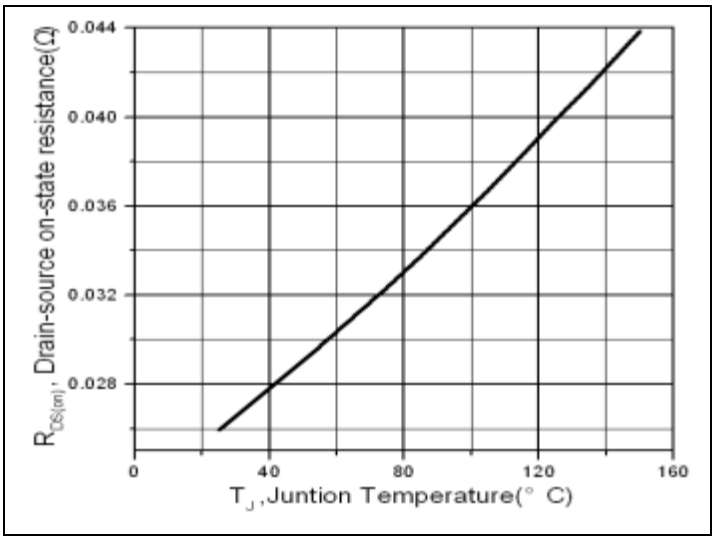


Figure1. Normalized On-Resistance vs. Case Temperature

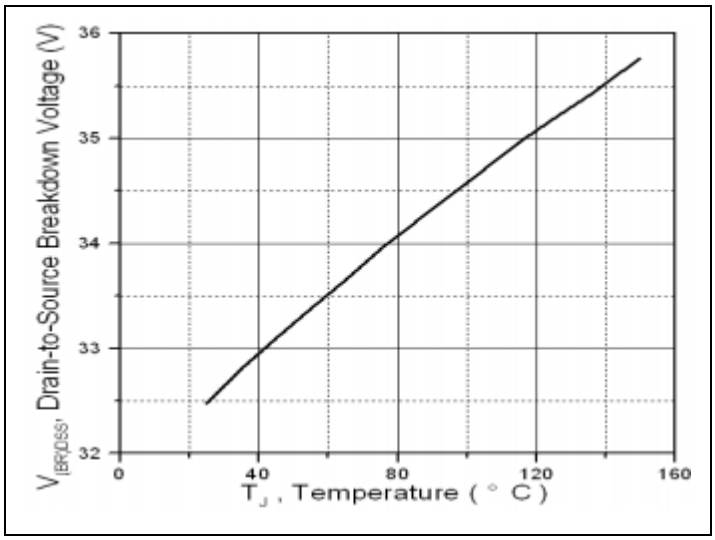


Figure2. Drain-to-Source Breakdown Voltage vs. Temperature

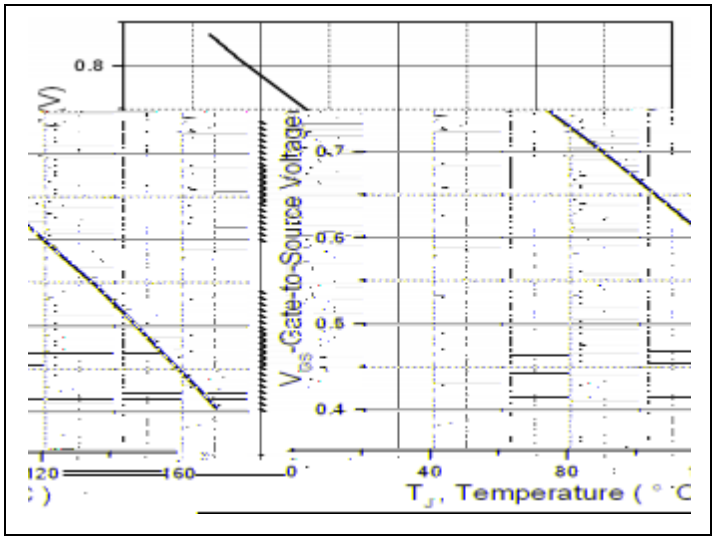


Figure3. Gate to Source Cut-off Voltage

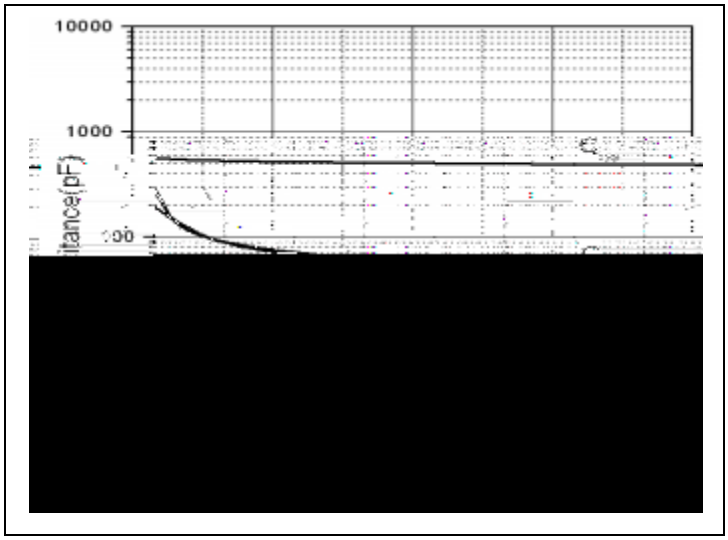
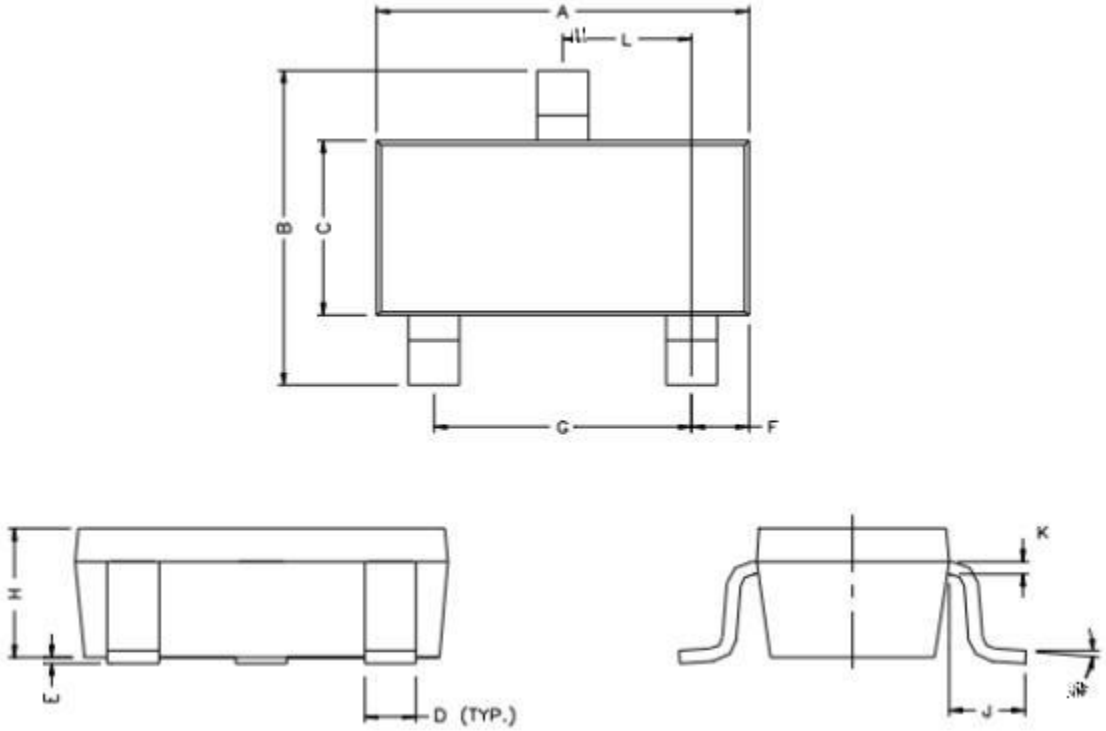


Figure 4. Typical Capacitance vs. Drain-to-Source Voltage

Mechanical Data：



REF.	Millimeter		REF.	Millimete	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0

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